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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/573,492	05/15/2006	Koichi Naniwae	8074-1143	9283
466	7590	08/24/2009	EXAMINER	
YOUNG & THOMPSON			JONES, ERIC W	
209 Madison Street				
Suite 500			ART UNIT	PAPER NUMBER
ALEXANDRIA, VA 22314			2892	
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			08/24/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/573,492	NANIWAE, KOICHI	
	<b>Examiner</b>	<b>Art Unit</b>	
	ERIC W. JONES	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 01 July 2009.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-57 is/are pending in the application.  
 4a) Of the above claim(s) 1,2,10,19,20,28 and 39-48 is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 3-9,11-18,21-27,29-38 and 49-57 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 15 May 2006 is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
     1. Certified copies of the priority documents have been received.  
     2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
     3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____ .                                    |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>7/8/2009 and 7/30/2009</u> .                                  | 6) <input type="checkbox"/> Other: _____ .                        |

**DETAILED ACTION**

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/1/2009 has been entered.

***Priority***

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 3-9, 11-18, 49, 50; and 53-57 are rejected under 35 U.S.C. 102(b) as being anticipated by Chiu et al (5,407,531).

Re claim 3, Chiu et al disclose in FIG. 1 a cleaning treatment method for eliminating contaminant adhered to the surface of a semiconductor layer, comprising:  
a cleaning treatment step of simultaneously providing a first gas including an etching agent (PCl<sub>3</sub>, AsCl<sub>3</sub>, Cl<sub>2</sub> or HCl) having an etching action with respect to the semiconductor layer (GaAs or InP layer 12) and a second gas including crystal growth

source material (trimethyl indium, TMIn) to the surface of the semiconductor layer, wherein the first gas and the second gas are supplied in an intermittent (ON/OFF cycles) manner, wherein an absolute value for a rate of change in thickness of the semiconductor layer during the cleaning treatment step is 0.1 nm/sec or less (0.1 to 3  $\mu\text{m}/\text{hr} = 0.0278$  to 0.83 nm/sec). (column 3, lines 20-68 and column 4, lines 1-52)

Re claim 4, Chiu et al disclose the first gas and the second gas are supplied intermittently for fixed periods of time, where a time of supplying the first and second gases and a time of not supplying the first and second gases are alternately repeated. (ON/OFF cycles) manner. (column 3, lines 65-68 and column 4, lines 1-52)

Re claims 5 and 55, Chiu et al disclose a difference in layer thickness of the semiconductor layer (GaAs or InP 12) before and after implementation of the cleaning treatment step is 100 nm or less. (ON/OFF cycles are repeated until desired thickness is achieved; column 4, lines 8-15)

Re claim 6, Chiu et al disclose layer thickness of the semiconductor layer is not substantially reduced during implementation of the step of subjecting the surface of the semiconductor layer to cleaning treatment. (ON/OFF cycles are repeated until desired thickness is achieved; column 4, lines 8-15)

Re claims 7, Chiu et al disclose the rate of change in layer thickness of the semiconductor layer is controlled by adjusting the quantitative ratio of the etching agent and the crystal growth source material. (column 3, lines 9-60)

Re claims 8, Chiu et al disclose a symbol for the rate of change of the layer thickness of the semiconductor layer is positive when the layer thickness increases and

is negative when layer thickness decreases; the rate of change of layer thickness of the semiconductor layer during implementation of the cleaning treatment step is R; a rate of change of layer thickness of the semiconductor layer in the case of supplying only the first gas to the semiconductor layer surface is  $r_1$  (etching), a rate of change of layer thickness of the semiconductor layer surface is  $r_2$  (growth); and the amount of the first gas and the second gas supplied is adjusted in such a manner that an absolute value for the rate of change of layer thickness becomes:  $|R| < |r_2| < |r_1|$ . (etch gas and growth gas can be adjusted such that you have either: 1. all etching,  $|r_2| = 0$ ; 2. mixed etching/growth with majority etching, where  $|r_2| < |r_1|$ ; 3. mixed etching/growth with majority growth; 4. all growth,  $|r_1| = 0$ ; column 3, lines 9-60)

Re claims 9, Chiu et al disclose  $R < 0$ . (GaAs or InP layer is decreased by etching during ON/OFF cycles until desired thickness is achieved; column 4, lines 8-15)

Re claim 11, Chiu et al disclose the crystal growth source material includes an element (indium, In and phosphorous, P) constituting the semiconductor layer (InP layer). (column 3, lines 49-60)

Re claim 12, Chiu et al disclose the crystal growth source material includes organic metal (trimethyl indium, TMIn). (column 3, lines 49-60)

Re claim 13, Chiu et al disclose the etching agent is a halogen compound ( $\text{PCl}_3$ ,  $\text{AsCl}_3$ ,  $\text{Cl}_2$  or  $\text{HCl}$ ). (column 3, lines 27-32)

Re claim 14, Chiu et al disclose the semiconductor layer is comprised of compound semiconductor (GaAs or InP). (column 3, lines 20-26)

Re claim 15, Chiu et al disclose the semiconductor layer is comprised of a group III-V compound (GaAs or InP) semiconductor. (column 3, lines 20-26)

Re claim 16, Chiu et al disclose the crystal growth source material is a compound (trimethyl indium, TMIn) including a group III element (indium, In) constituting the semiconductor layer (InP). (column 3, lines 49-60)

Re claim 17, Chiu et al disclose the group III element (indium, In) constituting the semiconductor layer (InP) is comprised of a single species. (column 3, lines 49-60)

Re claim 18, Chiu et al disclose the group III element constituting the semiconductor layer is indium (In). (column 3, lines 49-60)

Re claims 49 and 50, Chiu et al anticipates the limitations of the claims: The recitation of a concentration of residual Si of said surface of said semiconductor layer is a surface density of  $5 \times 10^{11}$  atoms/cm<sup>2</sup> or less discloses functional limitation.

The structure recited in Chiu et al is substantially identical to that of the claims, and was produced by substantially the same process, and Chiu et al disclose removing contaminants from the etched layer. Therefore, claimed properties or functions are presumed to be similar. See MPEP § 2112.02.

Re claim 53, Chiu et al disclose in FIG. 1 a cleaning treatment method for eliminating contaminant adhered to the surface of a semiconductor layer, comprising:  
a cleaning treatment step of simultaneously providing a first gas including an etching agent (PCl<sub>3</sub>, AsCl<sub>3</sub>, Cl<sub>2</sub> or HCl) having an etching action with respect to the semiconductor layer (GaAs or InP layer 12) and a second gas including crystal growth source material (trimethyl indium, TMIn) to the surface of the semiconductor layer,

wherein when it is taken that: a symbol for rate of change of layer thickness of the semiconductor layer is positive when layer thickness increases and is negative when layer thickness decreases; the rate of change of layer thickness of the semiconductor layer during implementation of the cleaning treatment step is R; a rate of change of layer thickness of the semiconductor layer in the case of supplying only the first gas to the semiconductor layer surface is  $r_1$  (etching), and a rate of change of layer thickness of the semiconductor layer in the case of supplying only the second gas to the semiconductor layer surface is  $r_2$  (growth), the amount of the first gas and the second gas supplied is adjusted in such a manner that an absolute value for the rate of change of layer thickness becomes:  $|R| < |r_2| < |r_1|$ . (etch gas and growth gas can be adjusted such that you have either: 1. all etching,  $|r_2| = 0$ ; 2. mixed etching/growth with majority etching, where  $|r_2| < |r_1|$ ; 3. mixed etching/growth with majority growth; 4. all growth,  $|r_1| = 0$ ; column 3, lines 9-60)

Re claim 54, Chiu et al disclose  $|R|$  is 0.1 nm/sec or less (0.1 to 3  $\mu\text{m}/\text{hr}$  = 0.0278 to 0.83 nm/sec). (column 3, lines 20-68 and column 4, lines 1-52)

Re claims 56 and 57, Chiu et al anticipates the limitations of the claims: The recitation of a concentration of residual Si of said surface of said semiconductor layer is a surface density of  $5 \times 10^{11}$  atoms/cm<sup>2</sup> or less discloses functional limitation.

The structure recited in Tsang is substantially identical to that of the claims, and was produced by substantially the same process, and Chiu et al disclose removing contaminants from the etched layer. Therefore, claimed properties or functions are presumed to be identical. See MPEP § 2112.02.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 21-27, 29-38, 51 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu et al.

Re claim 21, Tsang discloses a method of manufacturing a semiconductor device comprising the steps of:

forming a first semiconductor layer (GaAs or InP layer 12); subjecting the surface of the first semiconductor layer to cleaning treatment (etching with  $\text{PCl}_3$ ,  $\text{AsCl}_3$ ,  $\text{Cl}_2$  or HCl); and forming a second semiconductor layer (not shown; grown after etch) on the first semiconductor layer (12), wherein the step of subjecting the surface of the first semiconductor layer to cleaning treatment includes a step of simultaneously supplying a first gas including an etching agent ( $\text{PCl}_3$ ,  $\text{AsCl}_3$ ,  $\text{Cl}_2$  or HCl) having an etching action with respect to the semiconductor layer and a second gas including crystal growth source material (trimethyl indium, TMIn) to the surface of the semiconductor layer, wherein the first gas and the second gas are supplied in an intermittent (ON/OFF cycles) manner, and wherein an absolute value for a rate of change in thickness of the first semiconductor layer during the cleaning treatment step is 0.1 nm/sec or less (0.1 to 3  $\mu\text{m}/\text{hr} = 0.0278$  to 0.83 nm/sec). (column 3, lines 20-68 and column 4, lines 1-68 and column 5, lines 1-30)

Chiu et al fail to disclose at an upper part of a semiconductor substrate.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a semiconductor substrate with a layer(s) deposited at an upper surface prior to further device process as is evidenced by Tsang (5,346,581-prior art of record), column 5, lines 49-68

Re claim 22, Chiu et al disclose the first gas and the second gas are supplied intermittently for fixed periods of time, where a time of supplying the first and second gases and a time of not supplying the first and second gases are alternately repeated. (ON/OFF cycles) manner. (column 3, lines 65-68 and column 4, lines 1-52)

Re claim 23, Chiu et al disclose a difference in layer thickness of the semiconductor layer (GaAs or InP layer 12) before and after implementation of the cleaning treatment step is 100 nm or less. (ON/OFF cycles are repeated until desired thickness is achieved; column 4, lines 8-15)

Re claim 24, Chiu et al disclose layer thickness of the first semiconductor layer (12) is not substantially reduced during implementation of the step of subjecting the surface of the first semiconductor layer (12) to cleaning treatment. (ON/OFF cycles are repeated until desired thickness is achieved; column 4, lines 8-15)

Re claims 25, Chiu et al disclose the rate of change in layer thickness of the semiconductor layer is controlled by adjusting the quantitative ratio of the etching agent and the crystal growth source material. (column 3, lines 9-60)

Re claims 26, Chiu et al disclose a symbol for the rate of change of the layer thickness of the semiconductor layer is positive when the layer thickness increases and

Art Unit: 2892

is negative when layer thickness decreases; the rate of change of layer thickness of the semiconductor layer during implementation of the cleaning treatment step is R; a rate of change of layer thickness of the semiconductor layer in the case of supplying only the first gas to the semiconductor layer surface is  $r_1$  (etching), a rate of change of layer thickness of the semiconductor layer surface is  $r_2$  (growth); and the amount of the first gas and the second gas supplied is adjusted in such a manner that an absolute value for the rate of change of layer thickness becomes:  $|R| < |r_2| < |r_1|$ . (etch gas and growth gas can be adjusted such that you have either: 1. all etching,  $|r_2| = 0$ ; 2. mixed etching/growth with majority etching, where  $|r_2| < |r_1|$ ; 3. mixed etching/growth with majority growth; 4. all growth,  $|r_1| = 0$ ; column 3, lines 9-60)

Re claims 27, Chiu et al disclose  $R < 0$ . (GaAs or InP layer is decreased by etching during ON/OFF cycles until desired thickness is achieved; column 4, lines 8-15)

Re claim 29, Chiu et al disclose the crystal growth source material includes an element (indium, In and phosphorous, P) constituting the first semiconductor layer (InP layer). (column 3, lines 49-60)

Re claim 30, Chiu et al disclose the crystal growth source material includes organic metal (trimethyl indium, TMIn). (column 3, lines 49-60)

Re claim 31, Chiu et al disclose the etching agent is a halogen compound ( $PCl_3$ ,  $AsCl_3$ ,  $Cl_2$  or  $HCl$ ). (column 3, lines 27-32)

Re claim 32, Chiu et al disclose the first semiconductor layer is comprised of compound semiconductor (GaAs or InP). (column 3, lines 20-26)

Re claim 33, Chiu et al disclose the first semiconductor layer is comprised of a group III-V compound (GaAs or InP) semiconductor. (column 3, lines 20-26)

Re claim 34, Chiu et al disclose the crystal growth source material (trimethyl indium, TMIn) includes a a group III element (indium, In) constituting the first semiconductor layer (InP). (column 3, lines 49-60)

Re claim 35, Chiu et al disclose the group III element (indium, In) constituting the semiconductor layer (InP) is comprised of a single species. (column 3, lines 49-60)

Re claim 36, Chiu et al disclose the group III element constituting the semiconductor layer is indium (In). (column 3, lines 49-60)

Re claim 37, Chiu et al disclose the first semiconductor layer and the second semiconductor layer are formed using vapor phase epitaxy (Chemical Beam Epitaxy, CBE; column 1, lines 23-38).

Re claim 38, Chiu et al disclose a mask ( $\text{SiO}_2$ ) is formed on the first semiconductor layer (GaAs or InP layer 12) after the step of forming the first semiconductor layer, and after eliminating (patterning) the mask, the step of subjecting the surface of the first semiconductor layer to cleaning treatment is implemented. (column 2, lines 29-56)

Re claims 51 and 52, Chiu et al makes obvious the limitations of the claims: The recitation of a concentration of residual Si of said surface of said semiconductor layer is a surface density of  $5 \times 10^{11}$  atoms/cm<sup>2</sup> or less discloses functional limitation.

The structure recited in Chiu et al is substantially identical to that of the claims, and was produced by substantially the same process, and Chiu et al disclose removing

contaminants from the etched layer. Therefore, claimed properties or functions are presumed to be similar. See MPEP § 2112.02.

***Response to Arguments***

7. Applicant's arguments with respect to claims 3, 21 and 53 have been considered but are moot in view of the new ground(s) of rejection attributed to Chiu et al (5,407,531).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC W. JONES whose telephone number is (571)270-3416. The examiner can normally be reached on Monday-Friday 5:30AM-3:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571)272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Application/Control Number: 10/573,492  
Art Unit: 2892

Page 12

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Supervisory Patent Examiner, Art  
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Examiner, Art Unit 2892  
8/19/2009